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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,963	12/29/2003	Tzu-Shern Chen	250606-1040	7889

24504 7590 04/19/2007

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EXAMINER	
WHITE, DYLAN C	
ART UNIT	PAPER NUMBER
2819	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/748,963	CHEN ET AL.	
	Examiner	Art Unit	
	Dylan White	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-14* is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 1/2/2007 have been fully considered but they are not persuasive.

Regarding the Dangat reference, it is stated (col. 2 lines 53-55 & Fig. 2) that memory (102) may be implemented as an external memory. The memory (102) and the PLD may be each implemented on separate die. It is obvious that the two separate die can each be mounted in there own packages (as done with most semiconductor devices), and as Dangat discloses that the memory may be implemented as an external memory it would be in its own package because it's external to the PLD.

Even though Dangat states that "in one example" the memory could be mounted in the same package as the die containing the PLD, the Examiner has chosen the first option where the memory and PLD are formed on separate die and where the memory is external to the PLD (and therefore in its own package).

Therefore the rejection under 35 USC § 103(a) as follows still stands.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 6, are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangat (US. 6,507,213) in view of Harari et al. (US. 5,887,145).

Regarding claim 1, Dangat discloses a first printed circuit board (PCB) (100) having a socket (104) and a downloading unit (112); a field programmable gate array (116, col. 3, lines 1-4) disposed on the first PCB (100); a nonvolatile memory (102, col. 2, lines 46-47) storing program code for programming the FPGA (col. 2, lines 44); where the nonvolatile memory (102) downloads program codes thereof to the FPGA by the download unit (112).

Dangat fails to disclose the external memory is fixed by soldering to a second PCB.

The technique of soldering is well known in the art especially when dealing with programmable logic devices and Integrated Circuits. Soldering components on PCB's have been used with RAM, ROM, nonvolatile memory, processors, programmable gate arrays, configurable logic, capacitors, resistors, and many other electronic components; and have been used in PC, IC, FPGA and other PCB manufacturing techniques for 20+ years.

Harari teaches a nonvolatile memory (30) on a second PCB (20) plugged into a socket (14) of a first PCB (10), therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the FPGA and external memory circuit of Dangat and the second PCB as taught by Harari for providing expanded removable memory devices to the Integrated Circuit.

Regarding claim 2, Surface mount technology is well known to one or ordinary skill in the art, and it is inherent to solder SMT components to a PCB.

Regarding claim 6, the combination where the nonvolatile memory (102) is a flash memory (Dangat, col.2, lines 48-49).

Claims 3 and 4, are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangat (US. 6,507,213) in view of Harari et al. (US. 5,887,145) as applied to claims 1 above, and further in view of Ikezawa (US. 2005/0222300).

Regarding claim 3, the combination of Dangat and Harari teach that of claim 1, but fail to teach the nonvolatile memory as packaged in a COB package.

Ikezawa teaches package types including COB (par. 0195, line 15), therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the nonvolatile memory and FPGA of Dangat and Harari with the COB packages as taught by Ikezawa for the higher packed density of COB.

Regarding claim 4, the combination discloses package types including TSOP (Ikezawa, par. 0195, lines 6) and SOJ (Ikezawa, par. 0195, lines 5).

Claim 5, is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangat (US. 6,507,213) in view of Harari et al. (US. 5,887,145) as applied to claims 1 above, and further in view of Tsai (US. 6,028,319).

Regarding claim 5, the combination of Dangat and Harari teach that of claim 1, but fail to teach the nonvolatile memory as packaged in QFP, FQGP (aka PQFP), TQFP, or QFJ.

Tsai teaches the use of QFP (col. 2, line 2), PQFP (col. 1, line 64), TQFP (col. 2, line 4, and QFJ (col. 2, line 4), therefore, it would have been obvious to one of ordinary skill in the art at the time on invention to use the nonvolatile memory and FPGA of Dangat and Harari with the SMT chip packages taught by Tsai for cost competitive production of plastic packaging.

Claim 7, is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangat (US. 6,507,213) in view of Harari et al. (US. 5,887,145) as applied to claims 1 above, and further in view of Yee (US. 2003/0230799).

Regarding claim 7, the combination of Dangat and Harari teach that of claim 1, but fail to teach the nonvolatile memory as packaged in a BGA, or a fine pitch BGA.

Yee teaches the use of BGA and fine pitch BGA (par. 0054, lines 5-6), therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the nonvolatile memory and FPGA of Dangat and Harari with the SMT chip packages taught by Yee for more densely packed array area.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 8, the upgrade method comprising: removing the second printed circuit board circuit with the nonvolatile memory from the socket on the first PCB; disposing the second PCB with the nonvolatile memory on a writer; writing a new program into the nonvolatile memory by the writer; inserting the second printed circuit board with the nonvolatile memory into the socket, wherein the new program is stored in the nonvolatile memory; and downloading the new program stored in the nonvolatile memory to the FPGA by the downloading unit.

Regarding claim 9, as being dependent on claim 8.

Regarding claim 10, the first printed circuit board having a power put region and a plurality of I/O pin regions, where the power pin region is separated from the I/O pin regions and where each I/O terminal of the FPGA is electrically connected to a corresponding pin in the I/O pin region, all power terminals of the FPGA are electrically connected to pins in the power pin region, and pins in the power pin region and the I/O pin region are connected to external circuits through different connectors.

Regarding claims 11-14, as being dependent on claim 10.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dylan White whose telephone number is (571) 272-1406. The examiner can normally be reached on m-f 7:30- 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DW

RexfordBarnie

REXFORD BARNIE
SUPERVISORY PATENT EXAMINER

04/12/07